

FIG. 1A

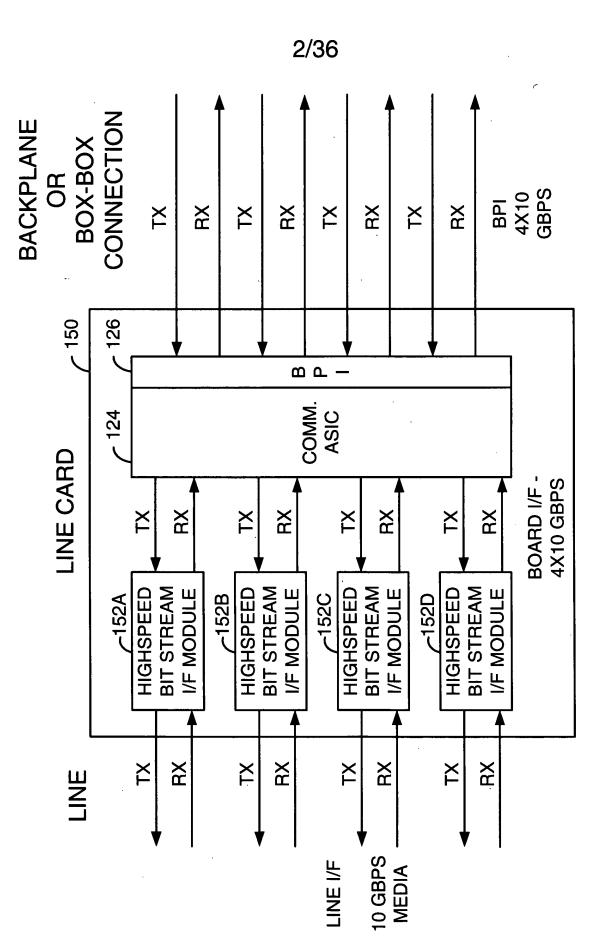


FIG. 1B

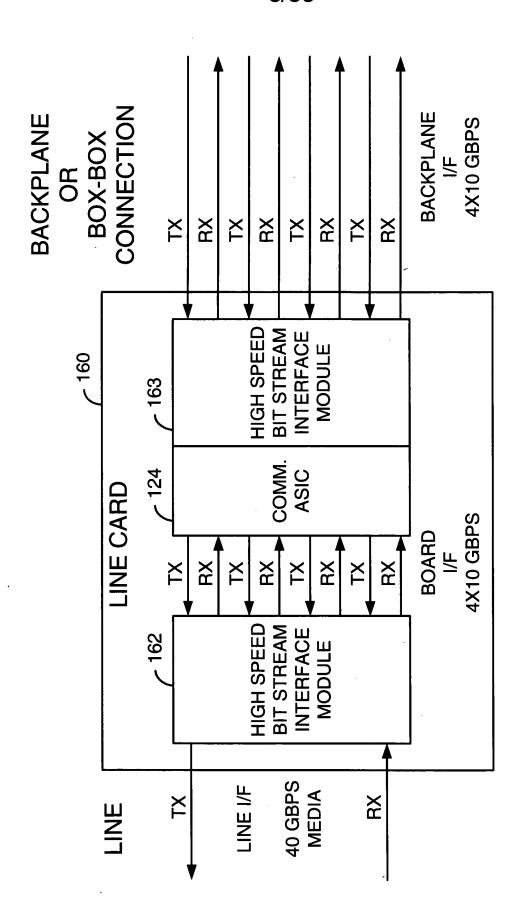


FIG. 1C

FIG. 1D

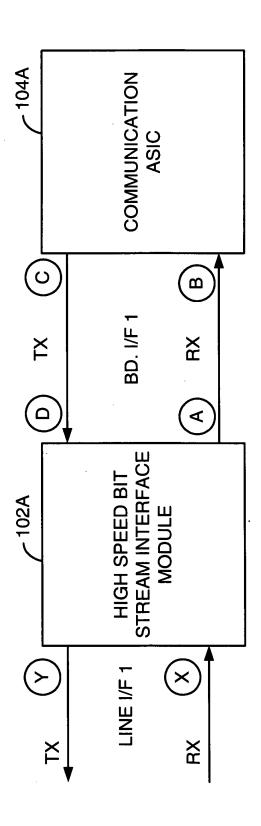
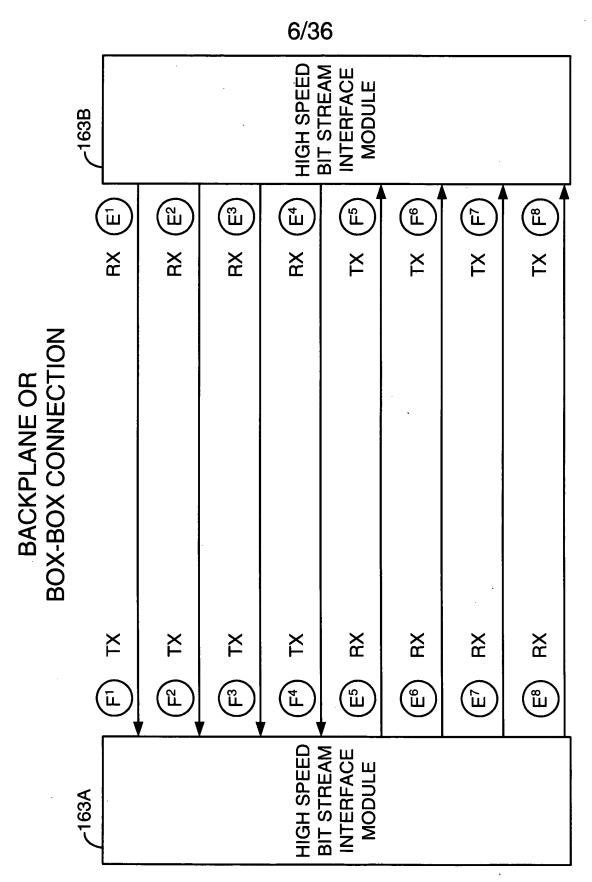


FIG. 2A



BACKPLANE I/F FI 4X10 GBPS

FIG. 2B

FIG. 3

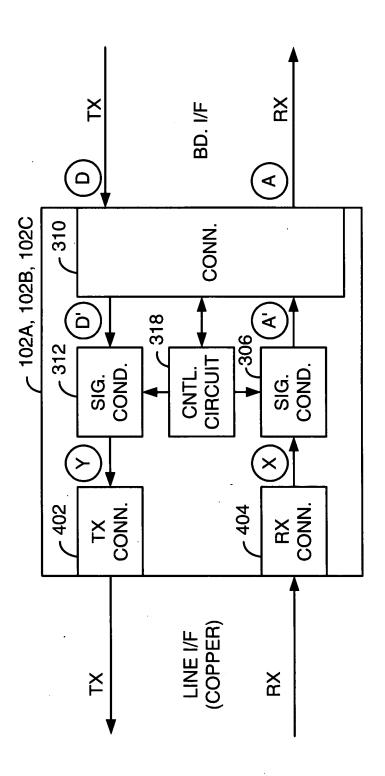


FIG. 4

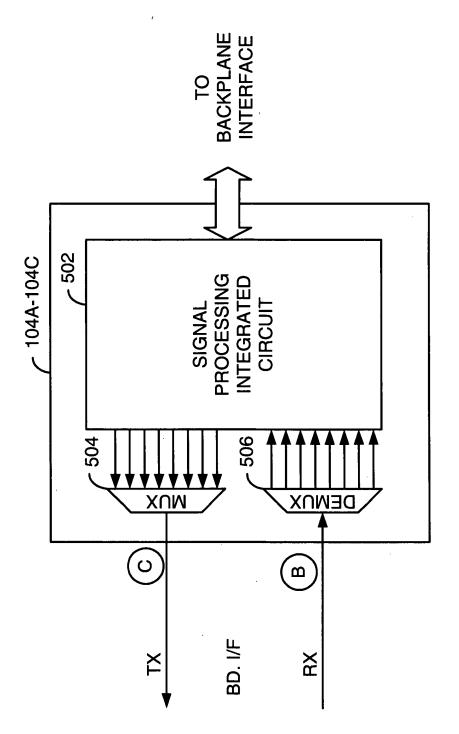
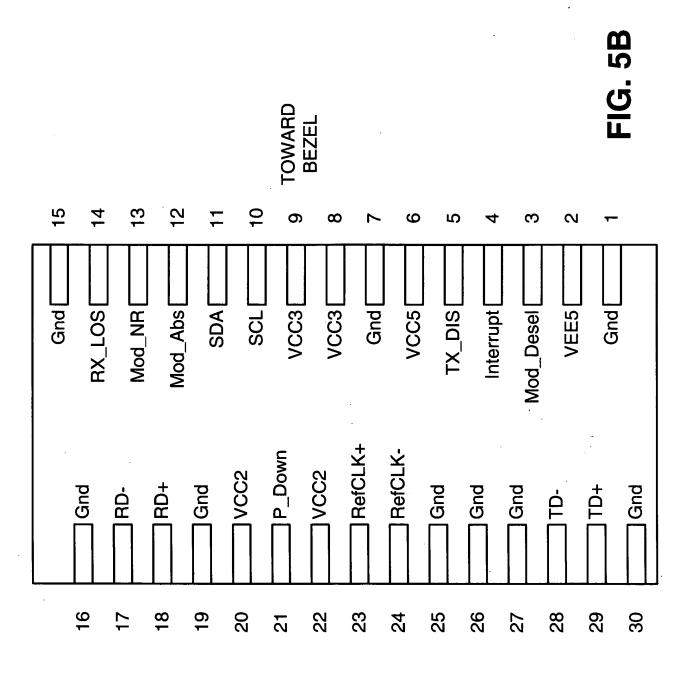


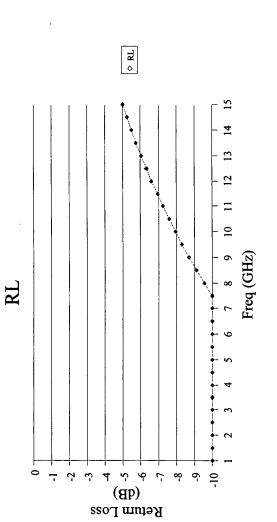
FIG. 5A



TOWARD ASIC

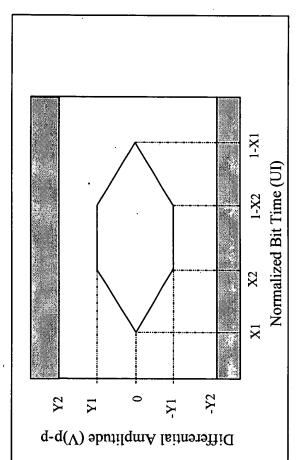
Parameter (Transmitter)	Symbol	Conditions	Min	Тур	Max	Typ Max Units
Single Ended Output Impedance	Zse		40	50	09	G
Differential Output Impedance	Z_{d}		80	100	120	Ω
Output Impedance Match	Z_{M}				10	%
CML output Amplitude, Diff., p-p	ΔVQDO			200	909	mV
Output Rise and Fall time (20% to 80%)	t _{RH} , t _{FH})	bs
			24	28	40	
Differential output return loss up	SII	Up to 7.5 GHz	·		-10	ф
		7.5-15 GHz			*	фВ
Single Ended output return loss	S11	Up to 15 GHz			-6	dВ
* $RL=-10+16.6 Log(f/7.5)$						





Parameter (Transmitter)	Symbol	Conditions	Min		Typ Max	Units
Nominal Bit Rate	f		9.95		10.75	GHz
Determinstic Jitter	DJ	MJS/802.3ae		0.12	0.12 0.15	UI
Random Jitter	R	MJS/802.3ae		0.13	0.13 0.15	III
Eye Mask	X1				0.15	III
Eye Mask	X2				0.4	II
Eye Mask	Y1				200	mV
Eye Mask	Y2	•			300	mV
SOENT Jitter (RMS)		Up to 80 MHz			10	mU

FIG. 5D



Parameter (Receiver)	Symbol	Conditions	Min	Тур	Min Typ Max	Units
Single Ended Input Impedance	ZeE		40	50	09	G
Differential Input impedance	Z		80	100	120	G
Input Impedance Match	Z				10	%
CML Input Differential Ampl., p-p	ΔΛΟΦΟ		125		1000	mV
Differential Input Return Loss	S22	Up to 7.5 GHz			-10	ф
		7.5-15 GHz		·	*1	dB
Single Ended Input Return Loss	S22	Up to 15 GHz			S-	dВ

1. RL=10 - 16.6 Log(f/7.5)

2. Single ended return loss is nessary for EMI.

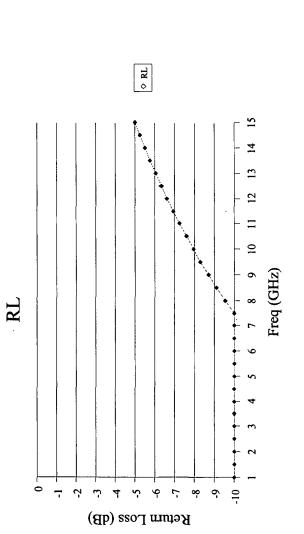
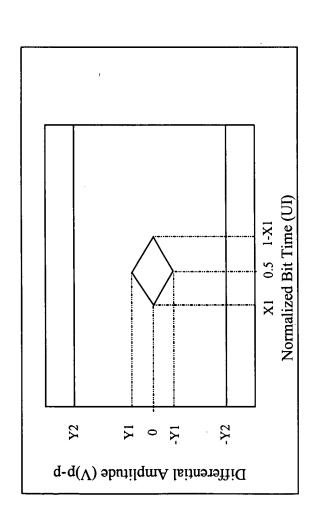
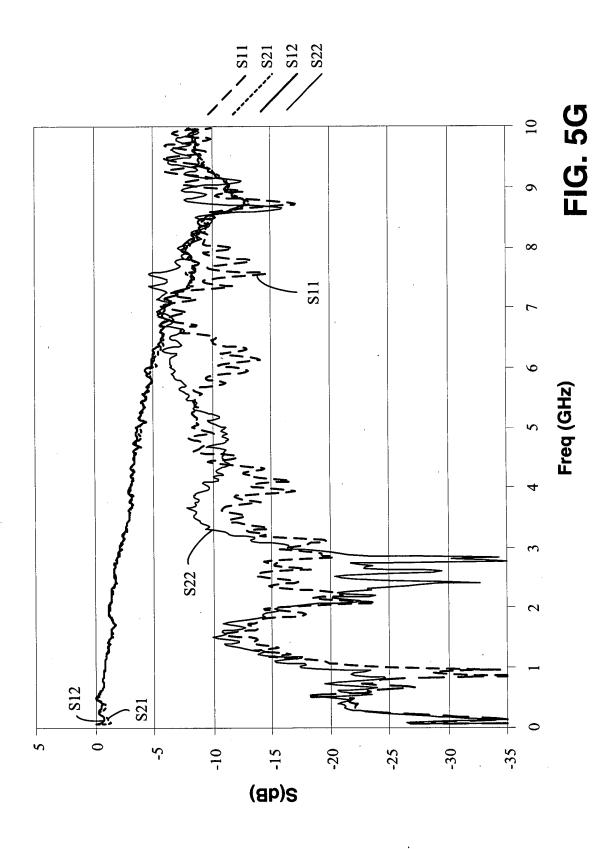


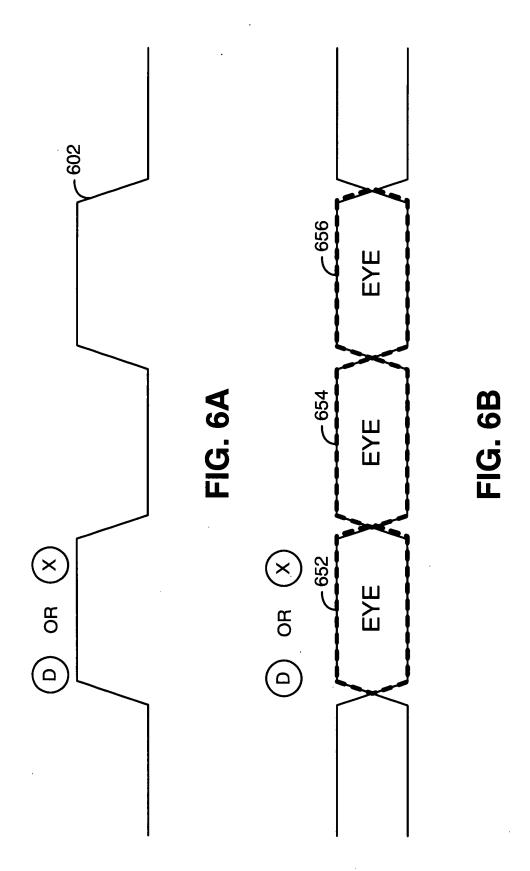
FIG. 5E

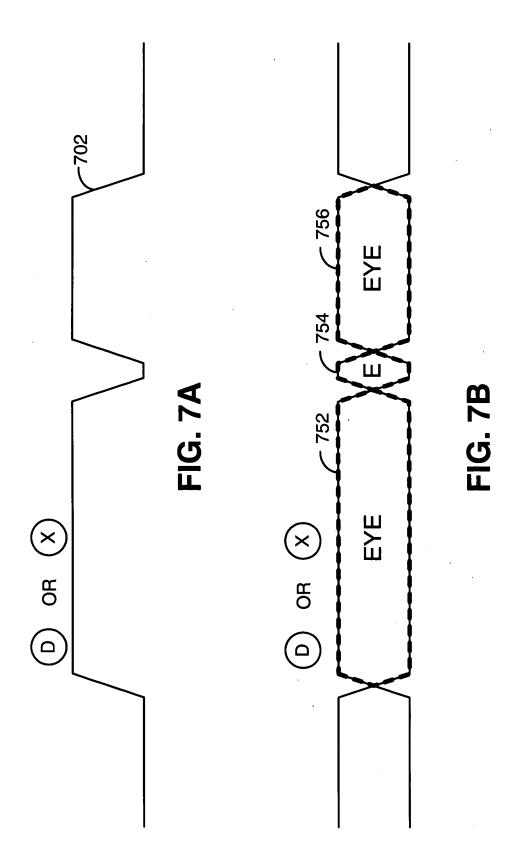
Parameter (Receiver)	Symbol	Conditions	Min	Тур	Min Typ Max	Units
Nominal Bit Rate	f		9.95		10.75	GHz
Determinstic Jitter *	DJ	MJS/802.3ae		0.35	0.35 0.55	UI
Random Jitter	RJ	MJS/802.3ae		0.18	0.2	UI
Eye Mask	X1				0.35	UI
Eye Mask	Y1				62.5	mV
Eye Mask	Y2				500	mV
SOENT Jitter		Up to 80 MHz			30	mU
* 0.25 UI of DJ is allocated to ISI from 8" of FR4 PCB trace.	of FR4 PCB	trace.				

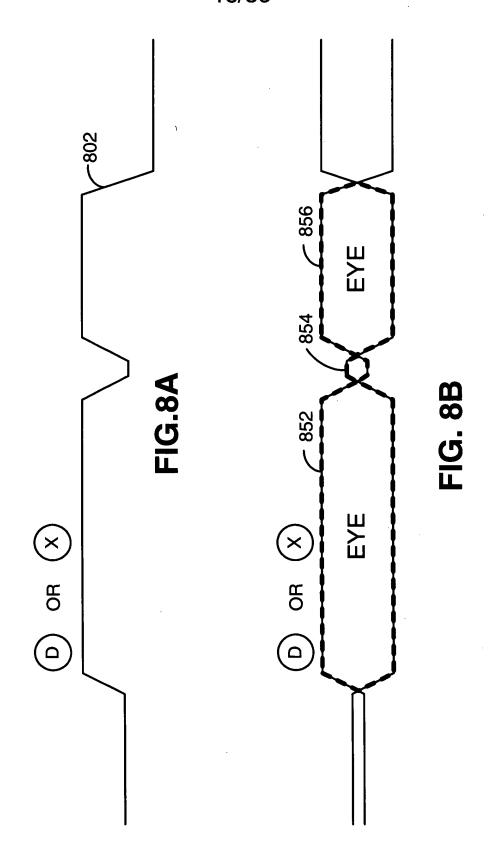
FIG. 5F

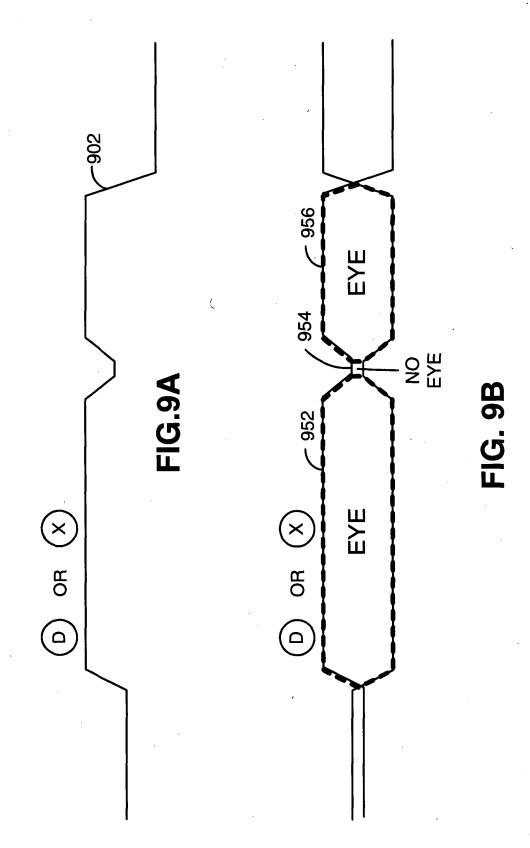












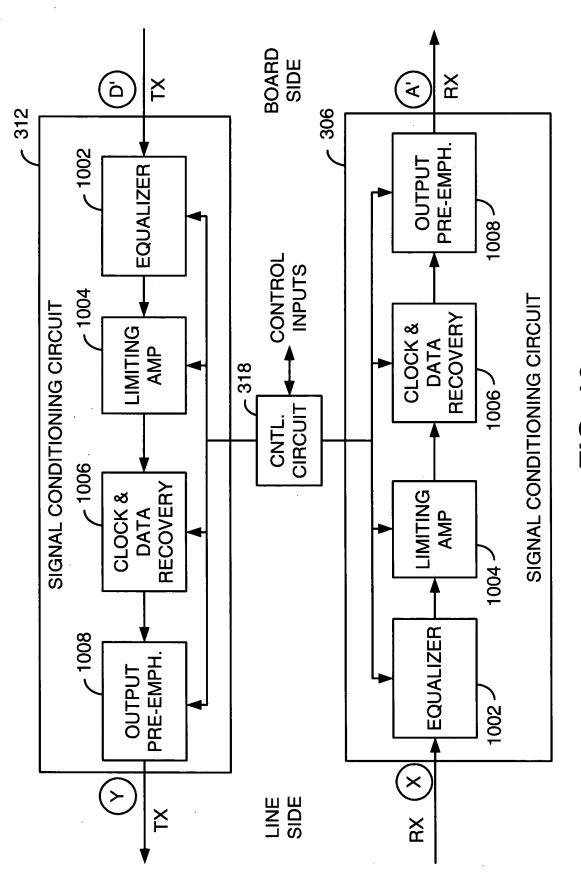
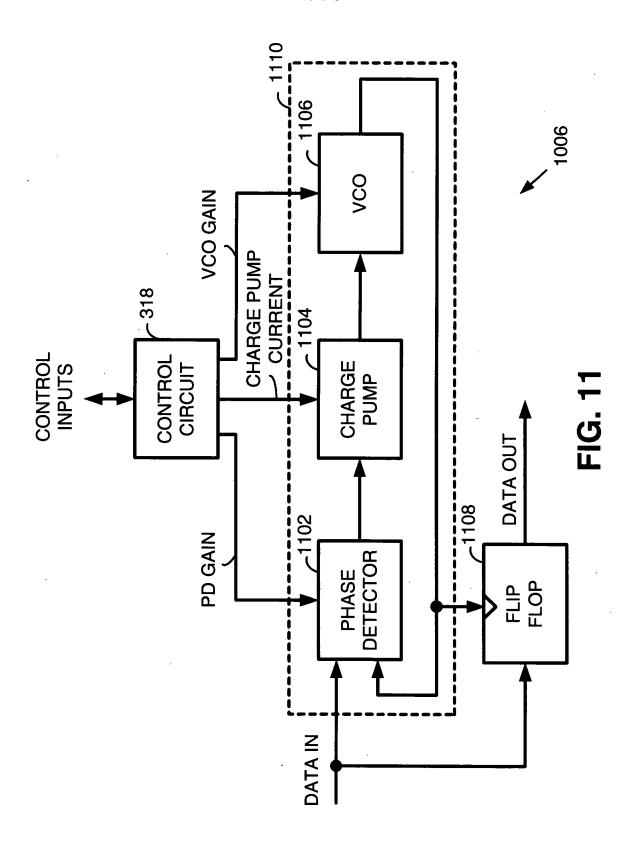


FIG. 10



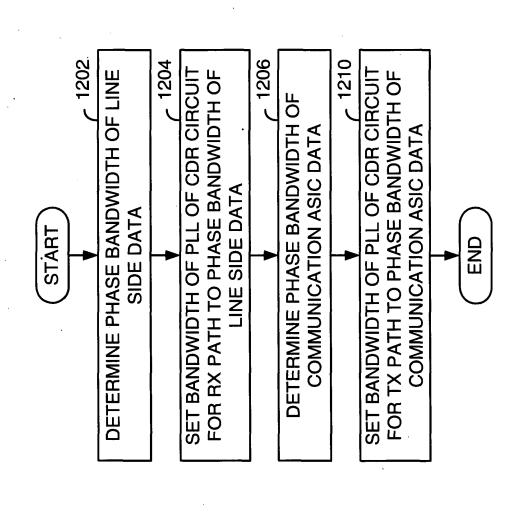


FIG. 12

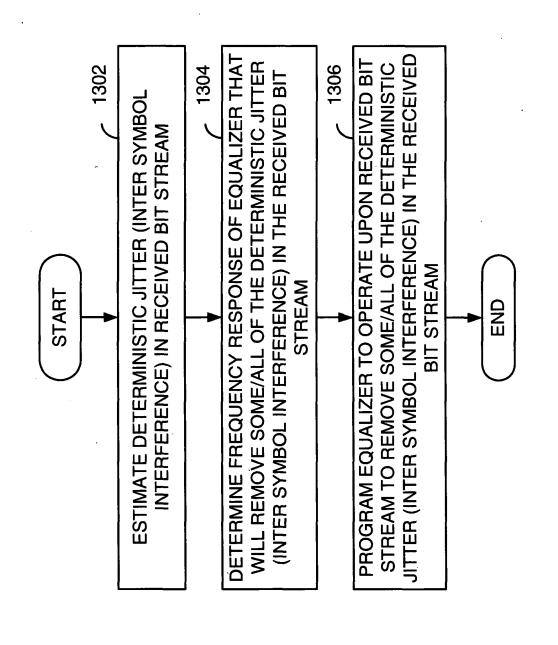
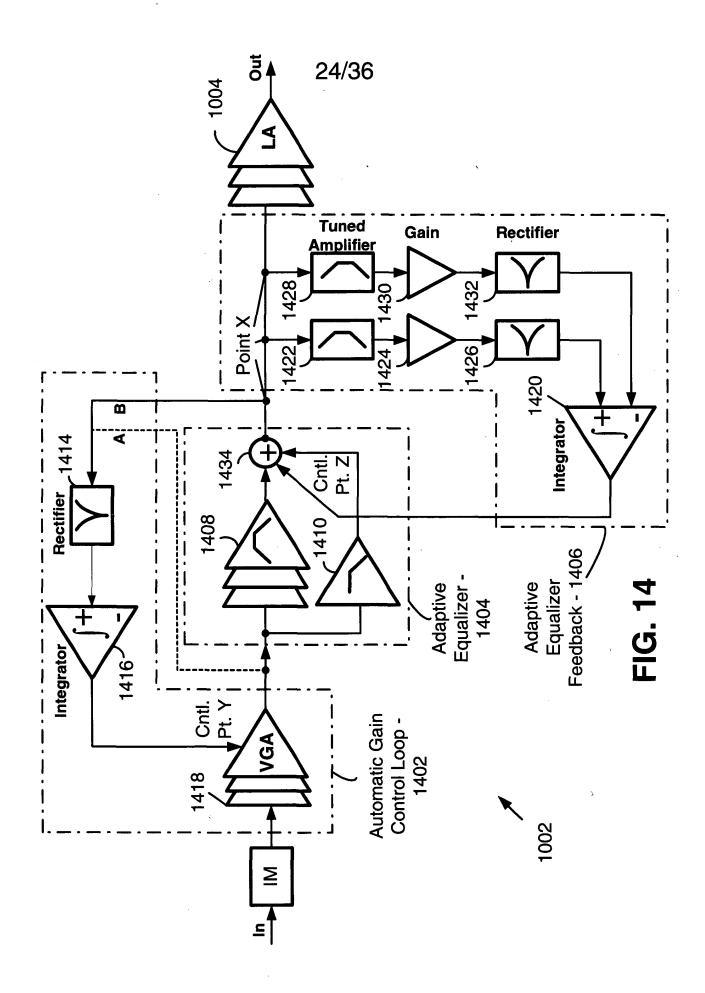
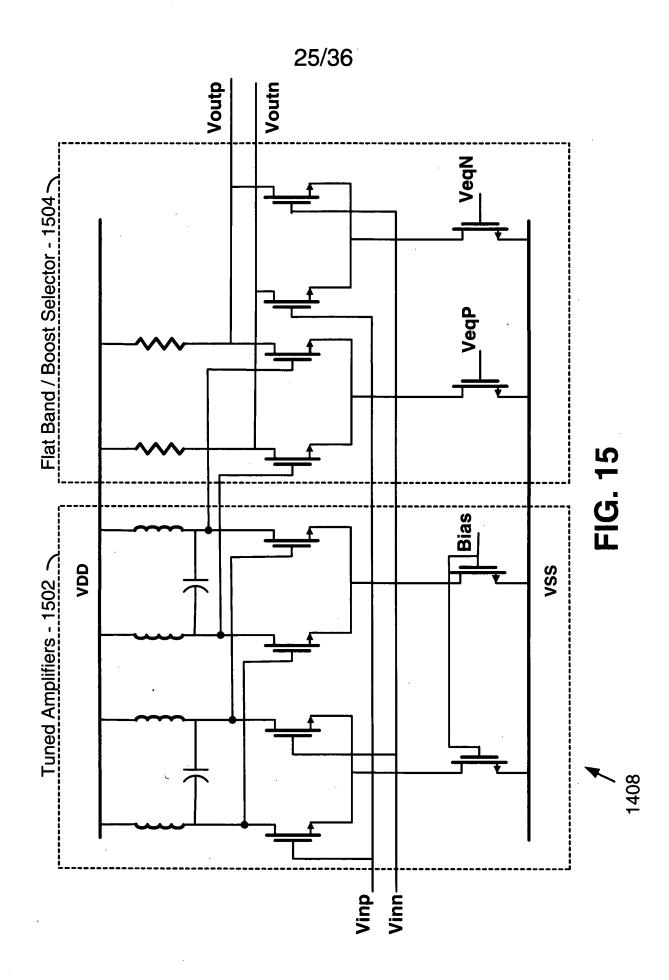
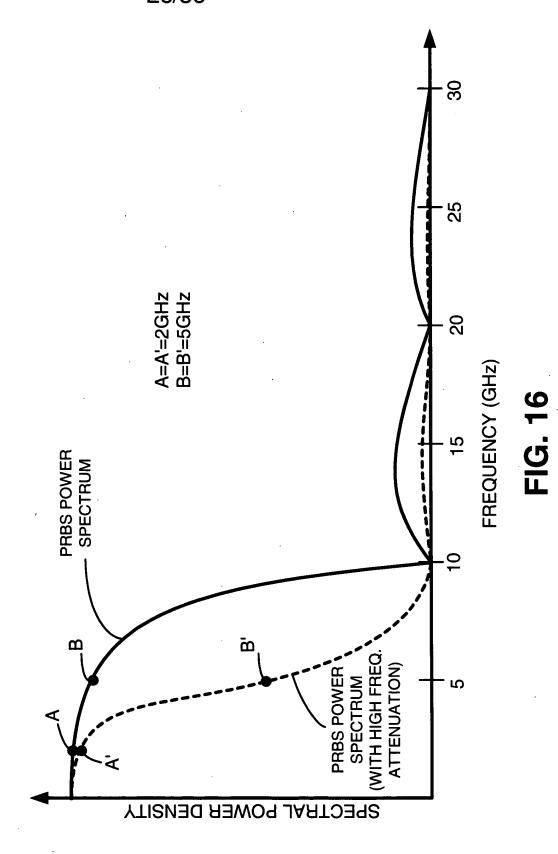
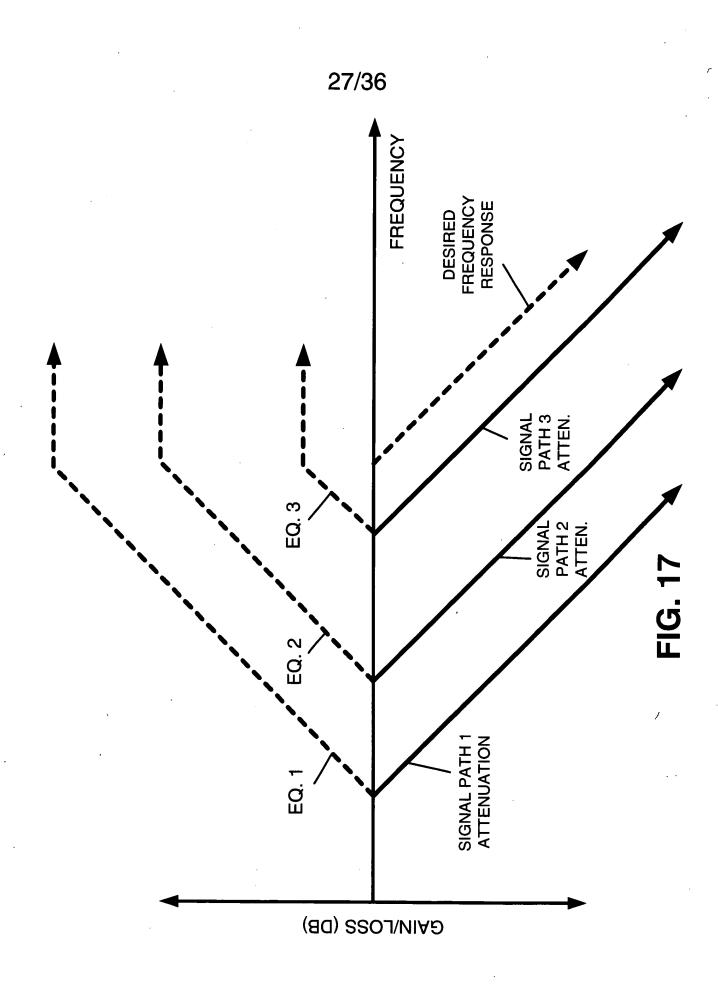


FIG. 13









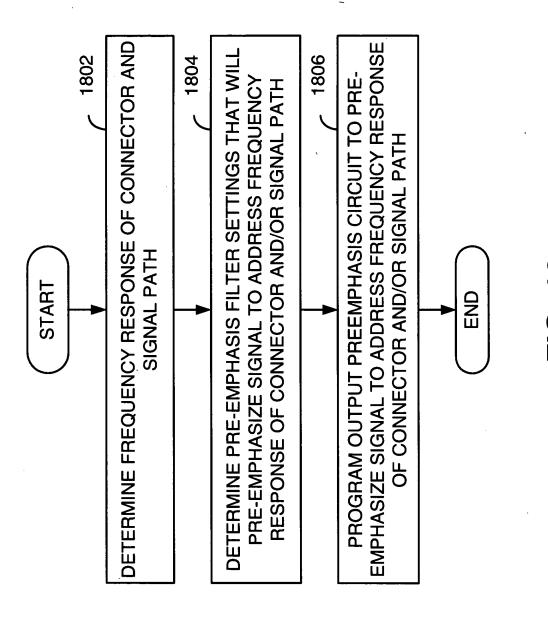


FIG. 18

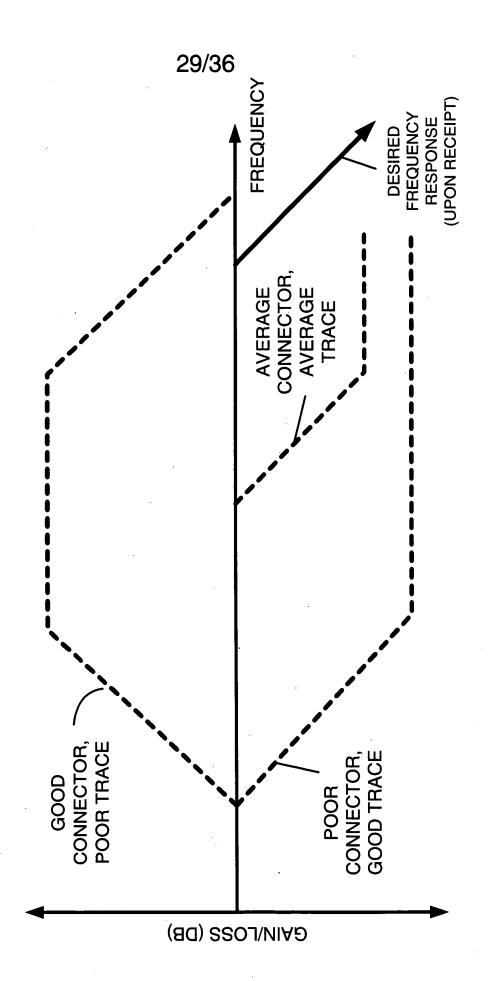


FIG. 19

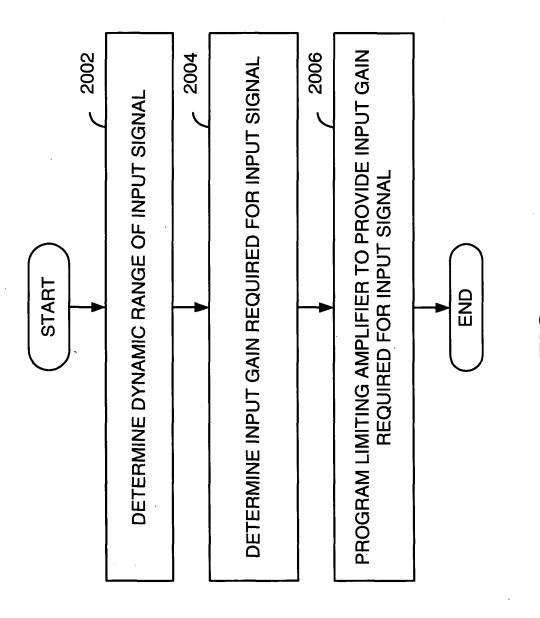


FIG. 20

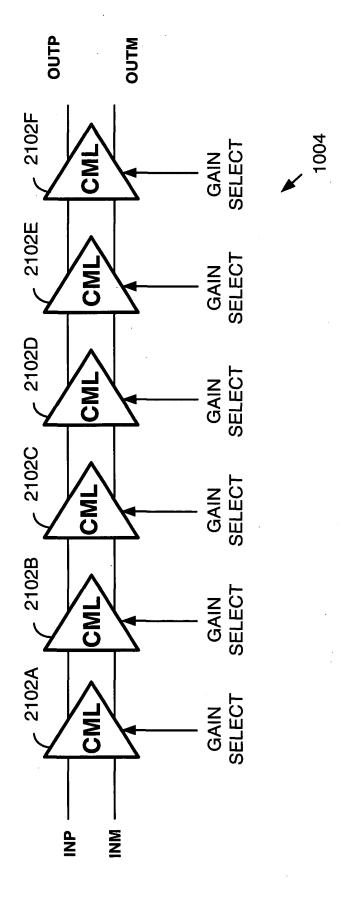
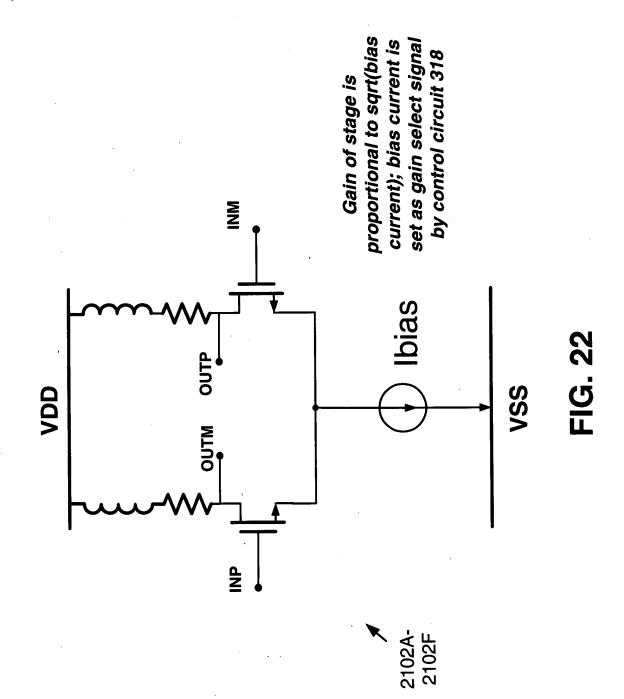
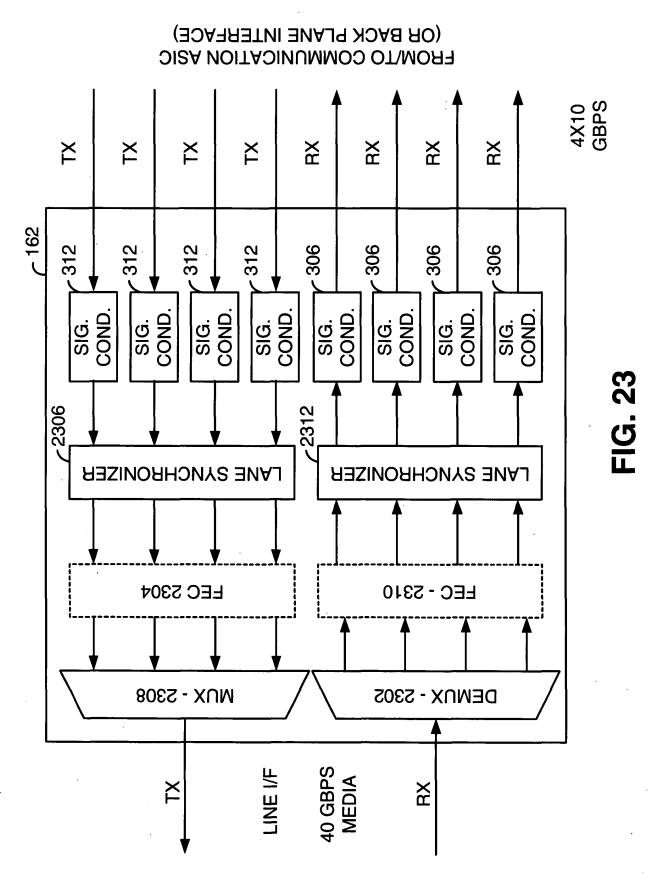


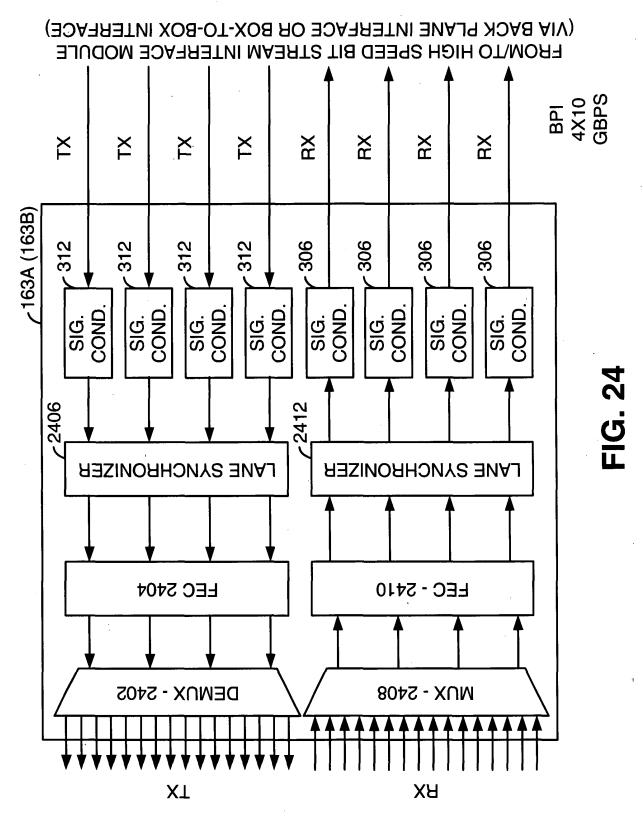
FIG. 21





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BOARD-SIDE INTERFACE



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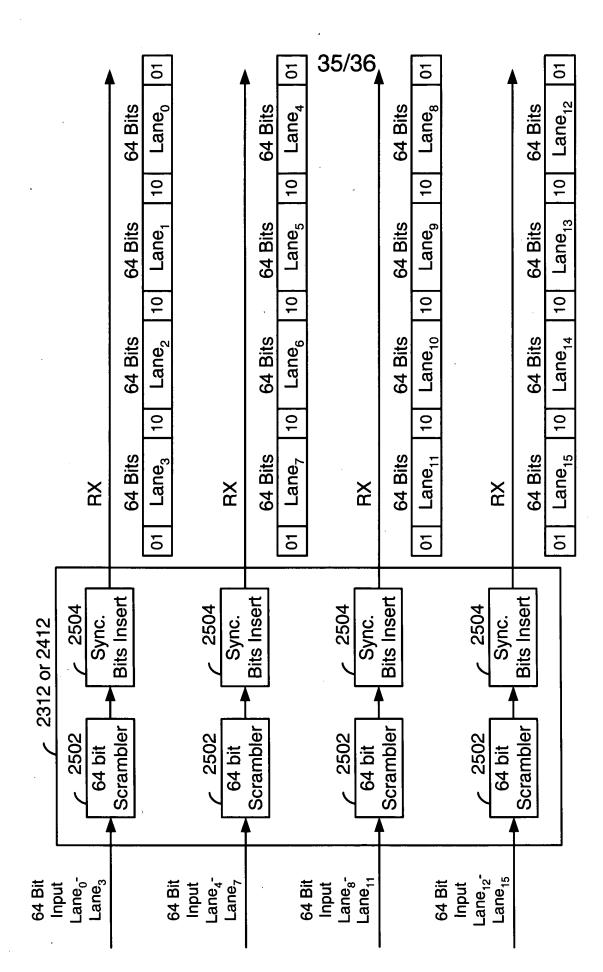


FIG. 25

